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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,187	07/12/2001	Richard C. Eden	IS9-018	3067

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WELLS ST. JOHN ROBERTS GREGORY & MATKIN P.S.
601 W. FIRST AVENUE
SUITE 1300
SPOKANE, WA 99201-3828

EXAMINER
FARAHANI, DANA

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/905,187	Applicant(s) EDEN ET AL.	
	Examiner Dana Farahani	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1, 3-13, 15-17, 19-22, 27, 30, 32, 34 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugawara et al., hereinafter Sugawara (U.S. Patent 4,794,441).

Regarding claims 1, 3-13 15-17, and 19-22, Sugawara discloses in figure 6 an integrated circuitry comprising a monolithic semiconductor substrate (not explicitly shown, but inherent to the circuit. See column 7, lines 4-21); a plurality of field effect transistors, hereinafter FET, G1 and G2, formed having plurality of electrical contacts including plurality of gate contacts (where the letter G is written), connected to each other, and a plurality of power contacts including source contacts and drain contacts, wherein the FETs are coupled in parallel with one another to form a power semiconductor switching device and wherein respective ones of the power contacts of the FETs are coupled in common with one another, as can be seen in the figure; and auxiliary circuitry, that is the circuitry which comprises elements 1, 5, 9, 14, 15, and 20, formed and coupled with at least one of the FETs, G2, further providing control signals to the gates. Also, note that Switch 1 could be said to be a convert power controller, a zero-current switching/time circuit, and a load protection circuit.

Regarding claim 27, although not shown in the figure, but if it was shown the in the detailed image of the transistors in the substrate the source and drains would be adjacent to the surface.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara, as applied to claim 1 above, and further in view of Kremlev et al., hereinafter Kremlev (U.S. Patent 4,175,240).

Sugawara does not expressly disclose planar field effect transistors and CMOS devices are used in the device. Kremlev teaches at column 3, lines 51-62 that planar FET transistors are used as switching transistors. Therefore, it would have been within the level of ordinary skill in the art to use planar field effect transistors, since it is well known in the art that planar FETs are commonly used as switching transistors.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara in view of Fujii (U.S. Patent 5,652,183).

Sugawara discloses the limitation in claim 18 except for the auxiliary circuitry comprises CMOS device. Fujii discloses at column 1, lines 25-34, the advantages of CMOS structures, which are well known in the art, such as faster speed and occupying

less chip area. Therefore, it would have been within the level of ordinary skill in the art to use a CMOS transistor instead of bipolar one used in Sugawara, since CMOS transistors can perform the same function as bipolar ones, but they occupy less space on the semiconductor chip structure and are faster.

6. Claims 23-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara as applied to claim 1 above, and further in view of Kalinsky et al., hereinafter Kalinsky (U.S. Patent 6,023,155).

Sugawara discloses the claimed invention, as discussed above, except for common source and drains of the two transistors.

Kalinsky discloses FET 315 of figure 3B is a power MOS transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use another transistor in parallel with G1 and G2, so it would have a common source/drain with one of G1 and G2, since parallel structure of the two identical transistors further enable control of current between the two nodes which are connected by the two transistors .

7. Claims 29, 31, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara as applied to claim 1 above, and further in view of Umeda et al., hereinafter Umeda (U.S. Patent 5,608,616).

Sugawara discloses the limitation in the claims, as discussed above, except for only n-channel transistors and a large number of transistors.

Umeda discloses in figure 5 power transistors in form of n-type transistors only, connected in parallel (see column 8, lines 52-63). Therefore, it would have been

obvious to one of ordinary skill in the art at the time of the invention to only use n-type transistors, since they are faster than p-type transistors. Although the two references do not disclose the exact number of transistors, it would have been obvious to one of ordinary skill in the art to use 5000 or more power transistors in the device, since the applicants have not disclosed that this cut-off number serves an specific purpose, or is for any particular reason, and it appears that the device perform equally well with a different number of transistors.

Response to Arguments

8. Applicant's arguments filed on 8/15/02 have been fully considered but they are not persuasive.

With regard to applicants' argument that the transistors in the primary reference operate as control devices, while in the invention of the instant application transistors are coupled to form power semiconductor switching device, the Office notes that a FET transistor in inherently a power switching device.

With regard to applicants' argument that claim 2 recites the field effect transistors comprise planar transistors, the Kremlev reference is used as an evidence to show the common usage of planar transistors, and replacing the vertical transistors of the Sugawara reference with planar transistors would have been obvious to one of ordinary skill in the art. Applicants argue that there is no motivation for combining the two references. However, the mere suitability of choosing the type of the transistor in an

otherwise previously known electronic device is within the level of ordinary skill in the art.

With regard to the rejection of claim 3, applicants argue that Sugawara fails to disclose or suggest the gate driver amplifier. However, shown in figure 6, gates of the transistors shown are connected to a gate driver, also shown in the figure. This same argument applies to applicants' argument that there is no zero current switching/timing or power converter controller, since these terms, while not explicitly defined in the specification, are broad enough so the circuitry in figure 6 of the reference reads on the terms.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
May 29, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800